IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Jonathan Kuppinger

Serial No.: 10/697,357
Filed: 29-October-2003
For: Method Of Partitioning An Integrated Circuit Desig

Group Art Unit: 2825
Examiner: Doan, Nghia M.
Atty Docket: 81610 / 03-1772

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Connie Del Castillo

7/21/06 Connie del Castillo

Date Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
(408) 433-8000

Date: 19 July 06

Respectfully submitted,

Timothy Croll

Reg. No.: 36,771